Refine Search

Search Results -

Terms	Documents
L2	0

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Search: L4

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Recall Text Clear Interrupt

Search History

DATE: Thursday, August 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L2	0	L4
L3	L2	0	L3
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same (processor or micrprocessor)	9	L2
L1	(macrocell or (macro adj1 cell)) same interfac$3 same bus	53	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 same (processor or micrprocessor)	9

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, August 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same (processor or micrprocessor)	9	L2
L1	(macrocell or (macro adj1 cell)) same interfac$3 same bus	53	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/253 |370/423 |370/463 |370/466 |370/257 |710/305 |710/300 |710/22 |710/52 |711/104 |712/10 |712/11 |712/13 |712/15 |712/32 |713/501 |713/502 |326/37 |326/38 |326/39 |326/40 |326/41 |326/62).ccls.	9389

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Search History

DATE: Thursday, August 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L1	710/305,300,22,52;370/423,463,466,257;326/37-41,62;713/501,502;712/10,11,13,15,32;709/253;711/104.ccls.	9389	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L1 and L2	35

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Search: L3

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Thursday, August 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	l1 and L2	35	L3
L2	(macrocell or (micro adj1 cell)) same interfac$3 same bus	54	L2
L1	710/305,300,22,52;370/423,463,466,257;326/37-41,62;713/501,502;712/10,11,13,15,32;709/253;711/104.ccls.	9389	L1

END OF SEARCH HISTORY

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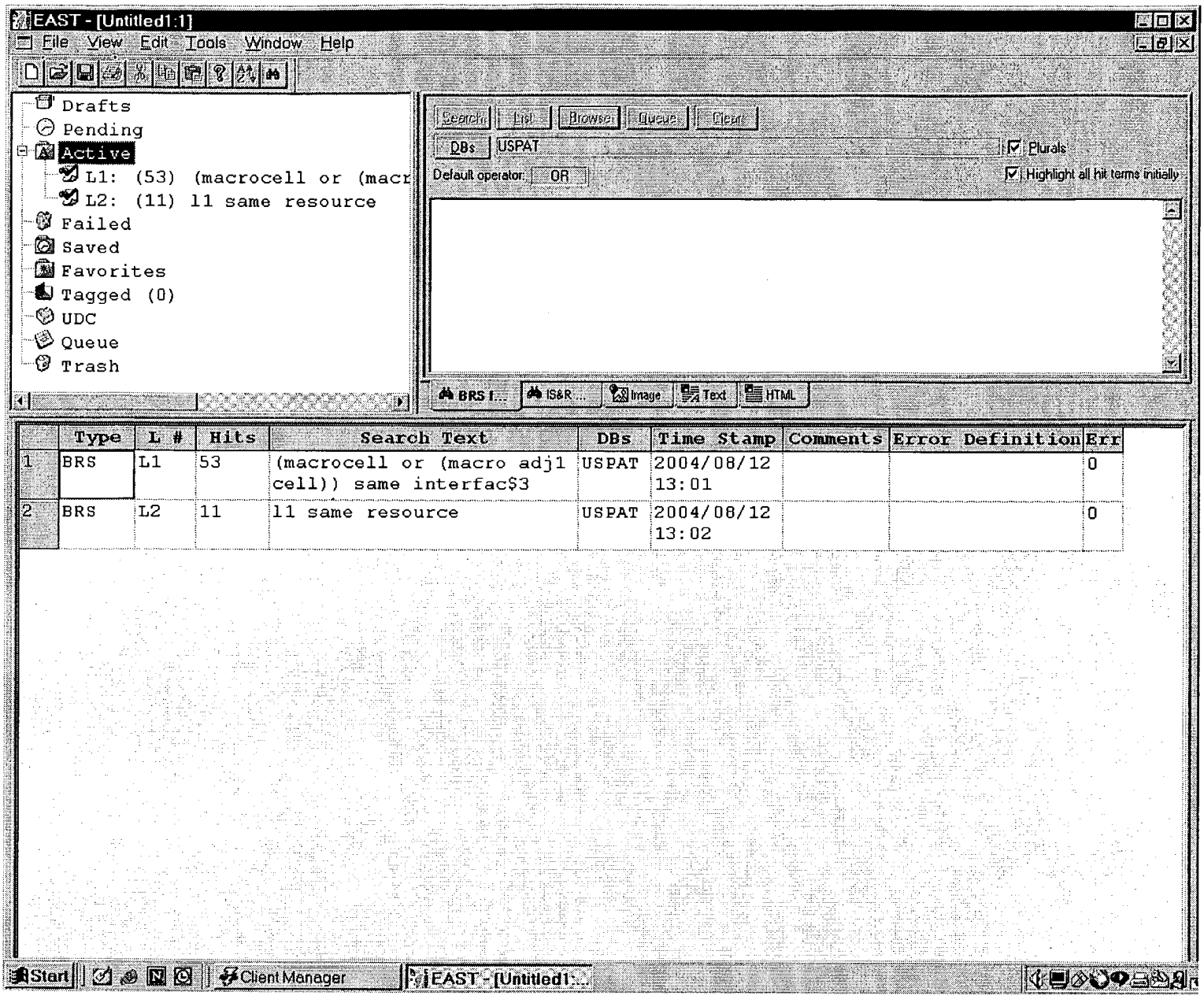
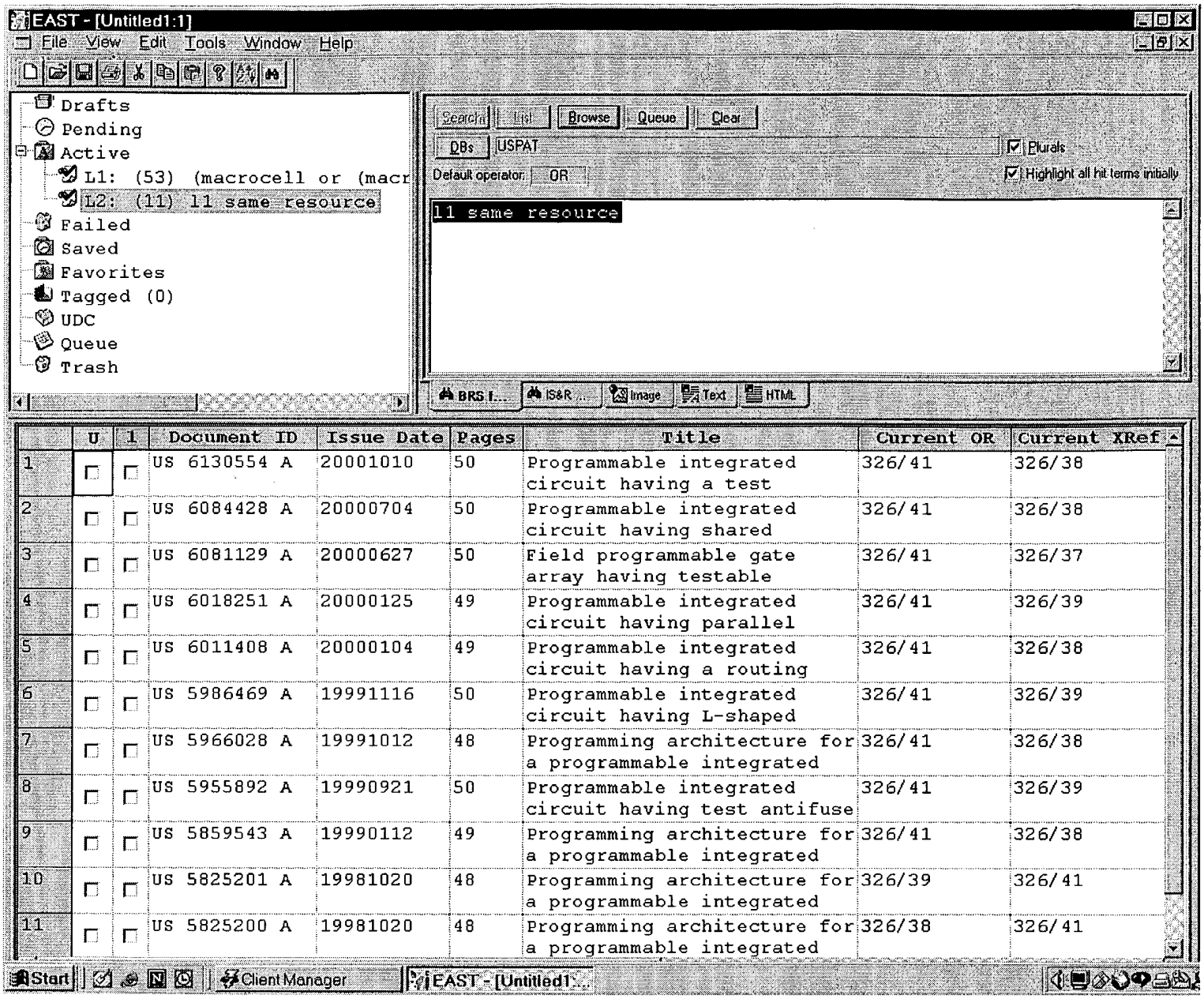


	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	53	(macrocell or (macro adj1 cell)) same interfac$3	USPAT	2004/08/12 13:01			0
2	BRS	L2	11	l1 same resource	USPAT	2004/08/12 13:02			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6130554 A	20001010	50	Programmable integrated circuit having a test	326/41	326/38
2	☐	☐	US 6084428 A	20000704	50	Programmable integrated circuit having shared	326/41	326/38
3	☐	☐	US 6081129 A	20000627	50	Field programmable gate array having testable	326/41	326/37
4	☐	☐	US 6018251 A	20000125	49	Programmable integrated circuit having parallel	326/41	326/39
5	☐	☐	US 6011408 A	20000104	49	Programmable integrated circuit having a routing	326/41	326/38
6	☐	☐	US 5986469 A	19991116	50	Programmable integrated circuit having L-shaped	326/41	326/39
7	☐	☐	US 5966028 A	19991012	48	Programming architecture for a programmable integrated	326/41	326/38
8	☐	☐	US 5955892 A	19990921	50	Programmable integrated circuit having test antifuse	326/41	326/39
9	☐	☐	US 5859543 A	19990112	49	Programming architecture for a programmable integrated	326/41	326/38
10	☐	☐	US 5825201 A	19981020	48	Programming architecture for a programmable integrated	326/39	326/41
11	☐	☐	US 5825200 A	19981020	48	Programming architecture for a programmable integrated	326/38	326/41

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(macro cell) and interfac* and bus Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A digital CMOS programmable clock generator**
Holler, P.T.; Lee, H.;
ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International , 19-23 Sept. 1994
Pages:280 - 287

[Abstract] [PDF Full-Text (620 KB)] **IEEE CNF**

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A digital CMOS programmable clock generator

Holler, P.T. Lee, H.
AT&T Bell Labs., Allentown, PA, USA ;

This paper appears in: **ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International**

Meeting Date: 09/19/1994 - 09/23/1994
Publication Date: 19-23 Sept. 1994
Location: Rochester, NY USA
On page(s): 280 - 287
Reference Cited: 3
Inspec Accession Number: 4998172

Abstract:
The digital CMOS software programmable clock generator (PCG) was designed as a **macro cell** to provide quadrature clocks for the Hobbit based Personal Communicators. The PCG produces a highly accurate variable frequency system clock from 20 kHz to 100 MHz (10 kHz to 50 MHz in quadrature), while using a single inexpensive crystal oscillator as a reference. Both the frequency and tolerance of PCG can be programmed by the user. This cell resides inside the system control chip and has a **bus interface** allowing local storage of programmed data. Control signals which start and stop operation come from a power management portion of the chip. The output frequency can be changed on

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Print Format

the fly

Index Terms:

20 kHz to 100 MHz CMOS digital integrated circuits Hobbit **bus interface** clocks crystal oscillator crystal oscillators digital CMOS **macro cell** output frequency personal communication networks personal communicators power management portion programmable clock generator pulse generators quadrature clocks system control chip variable frequency system clock 20 kHz to 100 MHz CMOS digital integrated circuits Hobbit **bus interface** clocks crystal oscillator crystal oscillators digital CMOS **macro cell** output frequency personal communication networks personal communicators power management portion programmable clock generator pulse generators quadrature clocks system control chip variable frequency system clock

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Search Results - Record(s) 1 through 10 of 35 returned.

☐ 1. Document ID: US 6707314 B2

Using default format because multiple data bases are involved.

L3: Entry 1 of 35 File: USPT Mar 16, 2004

US-PAT-NO: 6707314
DOCUMENT-IDENTIFIER: US 6707314 B2

TITLE: Integrated circuit device, electronic equipment, and method of placement of an integrated circuit device

DATE-ISSUED: March 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kasahara; Shoichiro	Minowa-machi			JP
Akiyama; Chisato	Himo			JP
Komatsu; Fumikazu	Okaya			JP

US-CL-CURRENT: 326/38; 326/39, 326/41, 716/17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6532511 B1

L3: Entry 2 of 35 File: USPT Mar 11, 2003

US-PAT-NO: 6532511
DOCUMENT-IDENTIFIER: US 6532511 B1

TITLE: Asochronous centralized multi-channel DMA controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 6442642 B1

L3: Entry 3 of 35 File: USPT Aug 27, 2002

US-PAT-NO: 6442642
DOCUMENT-IDENTIFIER: US 6442642 B1

TITLE: System and method for providing an improved synchronous operation of an

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advanced peripheral bus with backward compatibility

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 4. Document ID: US 6130554 A

L3: Entry 4 of 35 File: USPT Oct 10, 2000

US-PAT-NO: 6130554
DOCUMENT-IDENTIFIER: US 6130554 A

TITLE: Programmable integrated circuit having a test circuit for testing the integrity of routing resource structures

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 5. Document ID: US 6084428 A

L3: Entry 5 of 35 File: USPT Jul 4, 2000

US-PAT-NO: 6084428
DOCUMENT-IDENTIFIER: US 6084428 A

TITLE: Programmable integrated circuit having shared programming conductors between columns of logic modules

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 6. Document ID: US 6081129 A

L3: Entry 6 of 35 File: USPT Jun 27, 2000

US-PAT-NO: 6081129
DOCUMENT-IDENTIFIER: US 6081129 A

TITLE: Field programmable gate array having testable antifuse programming architecture and method therefore

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

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☐ 7. Document ID: US 6066961 A

L3: Entry 7 of 35 File: USPT May 23, 2000

US-PAT-NO: 6066961
DOCUMENT-IDENTIFIER: US 6066961 A

TITLE: Individually accessible macrocell

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 8. Document ID: US 6034545 A

L3: Entry 8 of 35 File: USPT Mar 7, 2000

US-PAT-NO: 6034545
DOCUMENT-IDENTIFIER: US 6034545 A

TITLE: Macrocell for data processing circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 6018251 A

L3: Entry 9 of 35 File: USPT Jan 25, 2000

US-PAT-NO: 6018251
DOCUMENT-IDENTIFIER: US 6018251 A

TITLE: Programmable integrated circuit having parallel routing conductors coupled to programming drivers in different locations

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 10. Document ID: US 6011408 A

L3: Entry 10 of 35 File: USPT Jan 4, 2000

US-PAT-NO: 6011408
DOCUMENT-IDENTIFIER: US 6011408 A

TITLE: Programmable integrated circuit having a routing conductor that is driven with programming current from two different programming voltage terminals

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L2	35

Display Format: - Change Format

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 11 through 20 of 35 returned.

☐ 11. Document ID: US 5986469 A

Using default format because multiple data bases are involved.

L3: Entry 11 of 35 File: USPT Nov 16, 1999

US-PAT-NO: 5986469
DOCUMENT-IDENTIFIER: US 5986469 A

TITLE: Programmable integrated circuit having L-shaped programming power buses that extend along sides of the integrated circuit

DATE-ISSUED: November 16, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Eaton; David D.	San Jose	CA		
Kolze; Paige A.	San Jose	CA		
Apland; James M.	Gilroy	CA		

US-CL-CURRENT: 326/41; 326/39

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 12. Document ID: US 5966028 A

L3: Entry 12 of 35 File: USPT Oct 12, 1999

US-PAT-NO: 5966028
DOCUMENT-IDENTIFIER: US 5966028 A

TITLE: Programming architecture for a programmable integrated circuit employing test antifuses and test transistors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 13. Document ID: US 5955892 A

L3: Entry 13 of 35 File: USPT Sep 21, 1999

US-PAT-NO: 5955892
DOCUMENT-IDENTIFIER: US 5955892 A
** See image for Certificate of Correction **

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TITLE: Programmable integrated circuit having test antifuse circuitry for testing programming conductors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 14. Document ID: US 5869981 A

L3: Entry 14 of 35 File: USPT Feb 9, 1999

US-PAT-NO: 5869981
DOCUMENT-IDENTIFIER: US 5869981 A

TITLE: High density programmable logic device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 15. Document ID: US 5864542 A

L3: Entry 15 of 35 File: USPT Jan 26, 1999

US-PAT-NO: 5864542
DOCUMENT-IDENTIFIER: US 5864542 A

TITLE: Scalable multimedia network

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 16. Document ID: US 5859543 A

L3: Entry 16 of 35 File: USPT Jan 12, 1999

US-PAT-NO: 5859543
DOCUMENT-IDENTIFIER: US 5859543 A

TITLE: Programming architecture for a programmable integrated circuit employing antifuses

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 17. Document ID: US 5834947 A

L3: Entry 17 of 35 File: USPT Nov 10, 1998

US-PAT-NO: 5834947
DOCUMENT-IDENTIFIER: US 5834947 A

TITLE: Microcontroller accessible macrocell

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

h e b b cg b cc e

☐ 18. Document ID: US 5825201 A

L3: Entry 18 of 35 File: USPT Oct 20, 1998

US-PAT-NO: 5825201
DOCUMENT-IDENTIFIER: US 5825201 A

TITLE: Programming architecture for a programmable integrated circuit employing antifuses

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 19. Document ID: US 5825200 A

L3: Entry 19 of 35 File: USPT Oct 20, 1998

US-PAT-NO: 5825200
DOCUMENT-IDENTIFIER: US 5825200 A

TITLE: Programming architecture for a programmable integrated circuit employing antifuses

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 20. Document ID: US 5799017 A

L3: Entry 20 of 35 File: USPT Aug 25, 1998

US-PAT-NO: 5799017
DOCUMENT-IDENTIFIER: US 5799017 A

TITLE: Scalable multimedia network

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L2	35

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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6735129 B2

Using default format because multiple data bases are involved.

L2: Entry 1 of 9 File: USPT May 11, 2004

US-PAT-NO: 6735129
DOCUMENT-IDENTIFIER: US 6735129 B2

TITLE: Semiconductor integrated circuit device

DATE-ISSUED: May 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Akasaki; Hiroshi	Ome			JP
Miyaoka; Shuichi	Hannou			JP
Yokoyama; Yuji	Ome			JP
Hasegawa; Masatoshi	Ome			JP
Kurita; Kozaburo	Ome			JP

US-CL-CURRENT: 365/194; 365/189.05, 365/189.08, 365/233

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6629288 B1

L2: Entry 2 of 9 File: USPT Sep 30, 2003

US-PAT-NO: 6629288
DOCUMENT-IDENTIFIER: US 6629288 B1

TITLE: Single clock cycle CRC engine

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 6532511 B1

L2: Entry 3 of 9 File: USPT Mar 11, 2003

US-PAT-NO: 6532511
DOCUMENT-IDENTIFIER: US 6532511 B1

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TITLE: Asochronous centralized multi-channel DMA controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 4. Document ID: US 6442642 B1

L2: Entry 4 of 9 File: USPT Aug 27, 2002

US-PAT-NO: 6442642
DOCUMENT-IDENTIFIER: US 6442642 B1

TITLE: System and method for providing an improved synchronous operation of an advanced peripheral bus with backward compatibility

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 5. Document ID: US 6345052 B1

L2: Entry 5 of 9 File: USPT Feb 5, 2002

US-PAT-NO: 6345052
DOCUMENT-IDENTIFIER: US 6345052 B1

TITLE: Method and apparatus for the reliable transition of status signals from an interface device when using a localized sampling architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 6. Document ID: US 6094726 A

L2: Entry 6 of 9 File: USPT Jul 25, 2000

US-PAT-NO: 6094726
DOCUMENT-IDENTIFIER: US 6094726 A

TITLE: Digital signal processor using a reconfigurable array of macrocells

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 7. Document ID: US 6064626 A

L2: Entry 7 of 9 File: USPT May 16, 2000

US-PAT-NO: 6064626
DOCUMENT-IDENTIFIER: US 6064626 A

TITLE: Peripheral buses for integrated circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

h e b b g e e e f e ef b e

☐ 8. Document ID: US 6034545 A

L2: Entry 8 of 9 File: USPT Mar 7, 2000

US-PAT-NO: 6034545
DOCUMENT-IDENTIFIER: US 6034545 A

TITLE: Macrocell for data processing circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Drawi De

☐ 9. Document ID: US 5832255 A

L2: Entry 9 of 9 File: USPT Nov 3, 1998

US-PAT-NO: 5832255
DOCUMENT-IDENTIFIER: US 5832255 A

TITLE: System and method for selecting a signal source to trigger a microprocessor counter/timer macro cell

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Drawi De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 same (processor or micrprocessor)	9

Display Format: - Change Format

Previous Page Next Page Go to Doc#

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L2: Entry 5 of 9 File: USPT Feb 5, 2002

DOCUMENT-IDENTIFIER: US 6345052 B1
TITLE: Method and apparatus for the reliable transition of status signals from an interface device when using a localized sampling architecture

Brief Summary Text (8):
Apart from the need for a simplified architecture for satisfying the timing requirements at the ATM-PHY interface, it will be appreciated by persons skilled in the art that the UTOPIA interface requires zero wait-state reaction to its input control signals. Routing delays at both the top-level and within each macro-cell can contribute to timing problems when interfacing the ATM layer with PHY layers. As a result, an ATM cell processor macro-cell must predict the next state of the input signals from the UTOPIA bus in order that the ATM cell processor can configure its outputs accordingly so as to avoid the possibility of incorrect predictions resulting in lost cells or FIFO overruns. If input control signals from the UTOPIA bus do not behave as predicted, a timing mechanism must be provided to ensure that the output status signals from the ATM cell processor continue to perform correctly in such circumstances. It would be advantageous if such a timing mechanism would extend to both single-channel and multi-channel implementations. It would be also advantageous if such a timing mechanism would enable the ATM-PHY interface device to maintain set-up and hold timing constraints that are much tighter than those required by the UTOPIA standard for the ATM-PHY interface. This would allow systems interfacing with the ATM-PHY interface device the flexibility of having more relaxed timing, thereby reducing design cycle time and the cost at both the device and system level.

Detailed Description Text (2):
Referring to FIG. 1, there is shown a known system for interfacing an ATM-PHY interface device 10 with other ATM layer devices (not shown) on the system-side 11 and with physical layer (PHY) links on the line-side 13. In the illustrative embodiment, ATM-PHY interface device 10 is a quad-channel device that interfaces, on the system side, with other ATM layer devices through an 8 or 16 bit wide UTOPIA bus and on the line-side, with up to four PHY layer devices. ATM-PHY interface device 10 includes a transmit-side 12 having four transmit cell processors 14, and a receive-side 16 having four receive cell processors 18. On transmit-side 12, each of transmit cell processors 14 is a macro-cell having its own transmit first-in first-out (FIFO) buffer (not shown) which provides FIFO management and a transmit cell interface to the line side transmission system of the subject transmit cell processor. Each transmit FIFO buffer can contain up to four ATM cells. The transmit FIFO buffers provide the cell rate decoupling function between the system-side ATM layer and the line-side transmission system connecting the PHY layers. Management functions of each transmit FIFO buffer include passing cells from the subject transmit FIFO buffer to its transmit cell processor for transmission to the corresponding PHY layer on line-side 13, indicating to the appropriate transmit cell processor when the subject transmit FIFO buffer is full, maintaining the read and write pointers of the subject transmit FIFO buffer and detecting a FIFO overrun condition. For each transmit cell processor, idle cells are automatically inserted into the line-side transmission stream when the corresponding transmit FIFO buffer contains less than one full cell. Each transmit cell processor 14 also optionally integrates circuitry to support ATM cell payload scrambling for cells read from the corresponding transmit FIFO buffer, header check sequence (HCS) generation, and

cell header scrambling.

Detailed Description Text (3):
In FIG. 1, the transmit cell processors 14 each contain sampling circuitry to sample the input signals from the UTOPIA bus 15. The redundant sampling circuitry makes meeting set-up and hold time constraints for the bus interface difficult to satisfy since physical routing in ATM-PHY device 10 of input signals from bus 15 is different for each of the transmit cell processors 14. Timing constraints are particularly problematic for a high speed bus, such as, for example, with the 50 MHz UTOPIA bus protocol which allows a maximum of 4 ns for input set-up and 1 ns for input hold. In addition to the top-level routing delay introduced by the redundant sampling circuitry in each transmit cell processor, the routing of signals within each transmit cell processor macro-cell may not be very deterministic thereby further adding to the difficulty in predicting the timing characteristics of signals, routed through device 10.

Detailed Description Text (4):
Referring to FIG. 2, there is shown an illustrative embodiment of an ATM-PHY interface device 20 having an improved architecture for simplifying the handling of UTOPIA interface requirements in accordance with the present invention. In ATM-PHY device 20 the sampling circuitry in each of transmit cell processors 22 has been removed and replaced with localized sampling circuitry 24 located at the top level of ATM-PHY device 20 between transmit cell processors (TXCPs) 22 and UTOPIA bus 26. In the illustrative embodiment, input signals from UTOPIA bus 26 are sampled by localized sampling circuitry 24 before being passed on to the appropriate ATM transmit cell processor macro-cells 22. The local sampling of UTOPIA input signals with sampling circuit 24 in ATM-PHY interface device 20 reduces the fan-out of signals which need to be sampled. Furthermore, since the sampling logic does not consist of as many logic gates as in the redundant sampling model in FIG. 1, the sampling logic can be preferably isolated into a small area of ATM-PHY interface device 20 and optimally placed thereby reducing the delay and the variability in the delay due to the physical layout of ATM-PHY interface device 20.

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First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
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L2: Entry 5 of 9 File: USPT Feb 5, 2002

US-PAT-NO: 6345052
DOCUMENT-IDENTIFIER: US 6345052 B1

TITLE: Method and apparatus for the reliable transition of status signals from an interface device when using a localized sampling architecture

DATE-ISSUED: February 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tse; Richard Tsz-Shiu	Vancouver			CA
McDowell; Shawn Patrick	Burnaby			CA

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
PMC-Sierra, Ltd.				CA	03

APPL-NO: 09/ 186159 [PALM]
DATE FILED: November 5, 1998

INT-CL: [07] H04 L 12/56

US-CL-ISSUED: 370/395.6; 370/465
US-CL-CURRENT: 370/395.6; 370/465

FIELD-OF-SEARCH: 370/230, 370/232, 370/235, 370/395, 370/423, 370/424, 370/463, 370/395.6, 370/465

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5784370	July 1998	Rich	370/395
☐	5889778	March 1999	Huscraft et al.	370/395
☐	6115360	September 2000	Quay et al.	370/235

OTHER PUBLICATIONS

The ATM Forum Technical Committee, "Utopia Specification Level 1, Version 2.01", Mar. 21, 1994.

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The ATM Forum Technical Committee, "Utopia Level 2, Version 1.0", Jun. 1995.

ART-UNIT: 2662

PRIMARY-EXAMINER: Kizou; Hassan

ASSISTANT-EXAMINER: Spafford; Tim

ATTY-AGENT-FIRM: Hall, Priddy, Myers & Vande Sande

ABSTRACT:

Method and apparatus are provided for guaranteeing that transmit cell available signals transmitted from an ATM-PHY interface device conform to a communication protocol. A previous transmit cell available signal from the previous clock cycle is stored and a transmit status signal and a transmit enable signal for the current clock cycle are sampled. One of the transmit status signal and the previous transmit cell available signal are selected as the new transmit cell available signal based upon the state of the transmit enable signal and the transmit status signal.

24 Claims, 18 Drawing figures

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L2: Entry 8 of 9 File: USPT Mar 7, 2000

DOCUMENT-IDENTIFIER: US 6034545 A
TITLE: Macrocell for data processing circuit

Brief Summary Text (5):
Typically, a data processing circuit such as a chip will include a number of macrocells that are arranged to interact with each other to perform data processing operations. Modular components such as the central processing unit, or processor core, used to apply instructions to data items read from memory, one or more caches or memories used to store instructions and data, a DMA bus master used to control activities such as data transfer, and an external memory interface for holding data to be output from the chip to memory, are examples of components which may be formed as macrocells.

Detailed Description Text (11):
The macrocell interface illustrated in FIG. 2 has separate input 210 and output 220 buses connected to input bus terminals 225 and 230, respectively. Data received at the input terminal 225 is passed over the input bus 210 to a buffer 235 which then passes that data over the path 260 to the processor core of the CPU 20. If the macrocell interface is incorporated in macrocells other than the CPU, then of course the macrocell logic receiving the data over path 260 will not be the processor core of the CPU, but will instead be the macrocell logic provided by that specific macrocell.

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L2: Entry 8 of 9 File: USPT Mar 7, 2000

US-PAT-NO: 6034545
DOCUMENT-IDENTIFIER: US 6034545 A

TITLE: Macrocell for data processing circuit

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Flynn; David Walter	Cambridge			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
ARM Limited	Cambridge			GB	03

APPL-NO: 09/ 015927 [PALM]
DATE FILED: January 30, 1998

INT-CL: [07] H03 K 19/177

US-CL-ISSUED: 326/39; 326/56, 326/82
US-CL-CURRENT: 326/39; 326/56, 326/82

FIELD-OF-SEARCH: 326/37-41, 326/56, 326/82, 326/83, 326/86

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5585742	December 1996	Kamiya	326/56
☐	5686844	November 1997	Hull et al.	326/46
☐	5705938	January 1998	Kean	326/41
☐	5850151	December 1998	Cliff et al.	326/39
☐	5880595	March 1999	Whetsel	326/40
☐	5894565	April 1999	Furtek et al.	326/38

ART-UNIT: 289

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PRIMARY-EXAMINER: Santamauro; Jon

ASSISTANT-EXAMINER: Le; Don Phu

ATTY-AGENT-FIRM: Nixon & Vanderhye P.C.

ABSTRACT:

The present invention provides a macrocell for a data processing circuit, comprising macrocell logic, and an interface for connecting the macrocell logic to a bus of the data processing circuit. The interface comprises: an input bus connected to an input bus terminal, an output bus connected to an output bus terminal, and a buffering circuit for buffering the output bus from the macrocell logic. Further, the interface has a mode input terminal for receiving a mode value, the mode value being arranged to control the buffering circuit. The buffering circuit is responsive to a first mode value to enter an inactive state when no data is being output from the macrocell, and is responsive to a second mode value to permanently drive the output bus. Hence, to enable the macrocell to be coupled to a unidirectional bus on the data processing circuit, the second mode value is supplied to the mode input terminal, whilst to enable the macrocell to be coupled to a bidirectional bus on the data processing circuit, the input bus terminal and output bus terminal are connected together externally to the macrocell, and the first mode value is supplied to the mode input terminal.

11 Claims, 4 Drawing figures

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L2: Entry 8 of 9 File: USPT Mar 7, 2000

US-PAT-NO: 6034545
DOCUMENT-IDENTIFIER: US 6034545 A

TITLE: Macrocell for data processing circuit

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Flynn; David Walter	Cambridge			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
ARM Limited	Cambridge			GB	03

APPL-NO: 09/ 015927 [PALM]
DATE FILED: January 30, 1998

INT-CL: [07] H03 K 19/177

US-CL-ISSUED: 326/39; 326/56, 326/82
US-CL-CURRENT: 326/39; 326/56, 326/82

FIELD-OF-SEARCH: 326/37-41, 326/56, 326/82, 326/83, 326/86

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5585742	December 1996	Kamiya	326/56
☐	5686844	November 1997	Hull et al.	326/46
☐	5705938	January 1998	Kean	326/41
☐	5850151	December 1998	Cliff et al.	326/39
☐	5880595	March 1999	Whetsel	326/40
☐	5894565	April 1999	Furtek et al.	326/38

ART-UNIT: 289

h e b b g e e e f c e e ge

PRIMARY-EXAMINER: Santamauro; Jon

ASSISTANT-EXAMINER: Le; Don Phu

ATTY-AGENT-FIRM: Nixon & Vanderhye P.C.

ABSTRACT:

The present invention provides a macrocell for a data processing circuit, comprising macrocell logic, and an interface for connecting the macrocell logic to a bus of the data processing circuit. The interface comprises: an input bus connected to an input bus terminal, an output bus connected to an output bus terminal, and a buffering circuit for buffering the output bus from the macrocell logic. Further, the interface has a mode input terminal for receiving a mode value, the mode value being arranged to control the buffering circuit. The buffering circuit is responsive to a first mode value to enter an inactive state when no data is being output from the macrocell, and is responsive to a second mode value to permanently drive the output bus. Hence, to enable the macrocell to be coupled to a unidirectional bus on the data processing circuit, the second mode value is supplied to the mode input terminal, whilst to enable the macrocell to be coupled to a bidirectional bus on the data processing circuit, the input bus terminal and output bus terminal are connected together externally to the macrocell, and the first mode value is supplied to the mode input terminal.

11 Claims, 4 Drawing figures

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L2: Entry 9 of 9 File: USPT Nov 3, 1998

DOCUMENT-IDENTIFIER: US 5832255 A
TITLE: System and method for selecting a signal source to trigger a microprocessor counter/timer macro cell

CLAIMS:

6. A system of macro cells in an integrated micro processor as in claim 5 wherein an external signal source having an output operatively connected to an external interface pin of the microprocessor provides a trigger signal, and in which said multiplexer has an external interface signal input operatively connected to the external signal source output via the external interface pin, said multiplexer selectively connecting said counter/timer gate input to the external source output in response to connection commands on the internal data bus.

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L2: Entry 9 of 9 File: USPT Nov 3, 1998

US-PAT-NO: 5832255
DOCUMENT-IDENTIFIER: US 5832255 A

TITLE: System and method for selecting a signal source to trigger a microprocessor counter/timer macro cell

DATE-ISSUED: November 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Roberts; Michael	Vancouver	WA		
Sabha; Raed	Vancouver	WA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sharp Microelectronics Technology, Inc.	Camas	WA			02
Sharp Kabushiki Kaisha	Osaka			JP	03

APPL-NO: 08/ 621118 [PALM]
DATE FILED: March 22, 1996

INT-CL: [06] G06 F 1/04

US-CL-ISSUED: 395/555; 395/557, 395/559
US-CL-CURRENT: 713/500; 713/502

FIELD-OF-SEARCH: 395/555, 395/557, 395/559, 395/560, 377/107, 377/111

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4348743	September 1982	Dozier	364/900
☐	4942522	July 1990	Wilkie et al.	395/557
☐	5535376	July 1996	Catherwood et al.	395/557
☐	5689690	November 1997	Lesmeister et al.	395/555

OTHER PUBLICATIONS

h e b b g e e e f c e e ge

Wescon Technical Papers, vol. 26, Sep. 1982, North Hollywood US, pp. 1-6, XP002034086, Patel R.: "The NS80CX48, a new CMOS, Single Chip Microcomputer for Critical Control and Low Power Appl."*p. 3, left-hand column, line 17--right-hand column, line 20; fig. 2,6.
Elektronik, vol. 38, No. 20, 29 Sep. 1989, pp. 84, 86-91, XP000067502, Alab M; "`Intelligente` Sensoren IM Automobil Bessere Daten Durch Integrierten mikrocontroller" pp. 87, right-hand column, line 32--pp. 88, right-hand column, line 2; fig. 5.
Wescon Technical Papers, vol. 27, 1983, North Hollywood US, XP002034087, Melear C.: "MC6805 Family Offers Multi-Function Capability", p. 5, left-hand column, line 4--p. 8, line 10, fig. 6.
MC68328 (DragonBall).TM. Integrated Processor User's Manual, .COPYRGT.Motorola, 1995; pp. 6-1 to 6-8, pp. 11-1 to 11-4.
Application Notes for 80C51-Based 8-Bit Microcontrollers; Philips Semiconductors, Jul. 1993; pp. 4-27 to 4-33.
1990 Single-Chip Microcontroller Data Book, NEC Electronics Inc., May 1990, Document No. 50053; pp. 7-3 to 7-19.
National Semiconductor, Advance Information, Sep. 1995, NS486.TM.SXF Optimized 32-Bit 486-Class Controller with On-Chip Periphals for Embedded Systems.
Article entitled RISC-Based Single-Chip Processor Targets PDAs, by Peter Fletcher in Electronic Design/Nov. 20, 1995, pp. 55-56, 60, 62, 64.

ART-UNIT: 277

PRIMARY-EXAMINER: Butler; Dennis M.

ATTY-AGENT-FIRM: Maliszewski; Gerald W. Ripma; David C.

ABSTRACT:

A system and method has been provided to selectively deliver a plurality of trigger signals to a counter/timer embedded in a microprocessor. The method provides the step of selecting a signal, from either internal or external sources, to trigger the counter/timer. If an internal source is selected, the method provides the step of selecting either a synchronous or non-synchronous signal source to trigger the counter/timer. Regardless of the source chosen, the method includes the step of generating a signal output from the selected source, and the further step of delivering the trigger signal on a dedicated connection. The method of the present invention also includes the step of counting clock cycles in response to the arrival of the trigger signal to the counter/timer. An apparatus to selectively deliver a trigger signal to a counter/timer embedded in a microprocessor from a plurality of signal sources is also provided. The apparatus includes an internal on-chip signal path extending between an internal PWM and the counter/timer, whereby the PWM can serve as the source of the trigger signal.

28 Claims, 6 Drawing figures

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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6122747 A

Using default format because multiple data bases are involved.

L5: Entry 1 of 1 File: USPT Sep 19, 2000

US-PAT-NO: 6122747
DOCUMENT-IDENTIFIER: US 6122747 A

TITLE: Intelligent subsystem interface for modular hardware system

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krening; Douglas N.	Larkspur	CO		
Lannan; Gregory B.	Larkspur	CO		
Schneiderwind; Michael J.	Castle Rock	CO		
Schneiderwind; Robert A.	Castle Rock	CO		
Caffrey; Robert T.	Silver Spring	MD		

US-CL-CURRENT: 713/323; 326/39, 326/41, 712/10, 712/11, 712/13, 712/15, 712/20, 712/32

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Terms	Documents
6122747.pn.	1

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US-PAT-NO: 6011408

DOCUMENT-IDENTIFIER: US 6011408 A

TITLE: Programmable integrated circuit having a routing conductor that is driven with programming current from two different programming voltage terminals

---- KWIC ---------

Brief Summary Text - BSTX (9):

A programming architecture for a programmable integrated circuit employing antifuses is disclosed. In one aspect, the number of programming conductors and the number of perpendicular programming control conductors for a-module are substantially equal in a particular macrocell architecture. In another aspect, programming current is supplied onto a long routing wire segment from two different programming conductors via-two programming transistors. In another aspect, a pattern of programming drivers alternates from one side of the integrated circuit to another from one column of macrocells to the next. In other aspects, control conductors and programming conductors are tested with test antifuses and test transistors. In another aspect, adjacent logic modules are mirrored so that they can share an intervening programming conductor resource. In another aspect, L-shaped programming power buses are provided and in another aspect, an express wire is simultaneously driven with programming current from two different programming voltage terminals. In another aspect, a test circuit is provided for testing the integrity of collinear routing wire segments in an unprogrammed programmable integrated circuit. In another aspect, programming transistors on the outputs of logic modules are tested. In another aspect, techniques and structures are disclosed for programming antifuses in interface cells that are disposed on branches of clock conductors.

US006011408A

United States Patent [19]

Kolze

[11] Patent Number: 6,011,408

[45] Date of Patent: Jan. 4, 2000

[54] **PROGRAMMABLE INTEGRATED CIRCUIT HAVING A ROUTING CONDUCTOR THAT IS DRIVEN WITH PROGRAMMING CURRENT FROM TWO DIFFERENT PROGRAMMING VOLTAGE TERMINALS**

[75] Inventor: **Paige A. Kolze, San Jose, Calif.**

[73] Assignee: **QuickLogic Corporation, Sunnyvale, Calif.**

[21] Appl. No.: **08/931,870**

[22] Filed: **Sep. 17, 1997**

Related U.S. Application Data

[62] Division of application No. 08/667,702, Jun. 21, 1996, Pat. No. 5,825,201.

[51] **Int. Cl.**[7] **H03K 19/177**

[52] **U.S. Cl.** **326/41; 326/38**

[58] **Field of Search** **326/38–41**

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,439,804	3/1984	Riddle et al.	361/92
4,758,745	7/1988	Elgamal et al. .	
4,857,774	8/1989	El-Ayat et al. .	
4,910,417	3/1990	El Gamal et al. .	
5,010,258	4/1991	Usami et al.	307/469
5,053,909	10/1991	Suzuki et al. .	
5,055,718	10/1991	Galbraith et al. .	
5,083,083	1/1992	El-Ayat et al. .	
5,132,563	7/1992	Fujii et al. .	
5,194,759	3/1993	El-Ayat et al.	307/202.1
5,196,724	3/1993	Gordon et al.	257/530
5,208,530	5/1993	El-Ayat et al. .	
5,220,213	6/1993	Chan et al.	307/465
5,243,226	9/1993	Chan .	
5,302,546	4/1994	Gordon et al.	437/170
5,304,871	4/1994	Dharmarajan et al. .	

(List continued on next page.)

OTHER PUBLICATIONS

Xilinx, "The Programmable Logic Data Book", pp. 8–11 through 8–36 (1994) no month.
S. Brown, et al., "Field Programmable Gate Arrays", pp. 1–43 and 88–202 (1992). No month.
S. Trimberger, "Field Programmable Gate Array Technology", pp. 1–14 and 98–170 (1994). No month.
D. Pellerin, et al., "Practical Design Using Programmable Logic", pp. 86–98 (1991). No month.
Advanced Micro Devices, PAL Device Book and Design Guide, pp. 2–236 through 2–247 (1993). (No month).
QuickLogic, Data Book, pp. 1–5 through 2–11 and 6–3 through 6–18 (1995) No month).
Actel, FPGA Data Book and Design Guide, pp. ix–xv, 1–5 through 1–34, 1–51 through 1–101, 1–153 through 1–222, 3–1 through 4–56 (1995). (No month).
Xilinx, "The Programmable Gate Array Design Hand Book", First Edition, pp. 1–9 through 2–73 (1986). No month.

Primary Examiner—Jon Santamauro
Assistant Examiner—Don Phu Le
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP

[57] **ABSTRACT**

A programmable integrated circuit (see FIG. 10) includes a routing conductor, i.e., "express wire," that extends substantially across the array of the integrated circuit. Because of the metal resistance through the long express wire, the express wire is simultaneously supplied with programming current from two different programming voltage terminals. Thus, programming current may be supplied to an electrode of an antifuse being programmed using programming current flowing through two separate programming voltage terminals. One programming voltage terminal supplies programming current via a first programming transistor and a first programming conductor to the express wire near one end of the programming conductor whereas another programming voltage terminal supplies programming current via a second programming transistor and a second programming conductor to the express wire near an opposite end of the express wire. The programming drivers that drive the first and second programming conductors are disposed adjacent opposite sides of the integrated circuit.

5 Claims, 39 Drawing Sheets